Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1 (currently amended): A pulse width control system comprising:

a serial transmission line for receiving serial data signals;

a differential pair having a first transistor and a second transistor, the first and second transistors being connected to the transmission line for respectively producing a positive data signal and a negative data signal, the first transistor being controlled by a first control signal and the second transistor being controlled by a second control signal, a differential data signal being produced by subtracting the negative data signal from the positive data signal;

a first delay control cell connected to the first transistor for delaying the first control signal;

a second delay control cell connected to the second transistor for delaying the second control signal;

wherein delay times caused by the first and second delay control cells to delay the first and second control signals are adjusted to ensure that all data pulses of the differential data signal have uniform width, when a status of the serial transmission line remains in a transmit mode, the first and second delay control cells generate a first delay time, and when a status of the serial transmission line switches from an idle mode to the transmit mode, the first and second delay control cells generate a second delay time, the first and second delay times being unequal.

2-3 (cancelled).

4 (currently amended): The system of ~~claim 3~~ claim 1 wherein the second delay time is

larger than the first delay time.

5 (currently amended): The system of ~~claim 3~~ claim 1 wherein the second delay time is generated to delay exactly one data pulse after the serial transmission line switches ~~switch~~ from the idle mode to the transmit mode.

6 (currently amended): The system of claim 1 wherein the first and second delay control cells each comprises ~~comprise~~ controllable resistor strings for providing delay times.

7 (cancelled).

8 (currently amended): The system of claim 1 wherein the first and second delay control cells ~~comprise~~ each comprises logic circuitry, and delay times are produced by propagation delays of the logic circuitry.

9 (currently amended): The system of claim 1 wherein the first and second delay control cells each ~~comprise~~ comprises a control transistor, and delay times are produced by varying voltage levels of signals that control the control ~~transistors~~ transistor in order to change channel widths of the control ~~transistors~~ transistor.

10 (new): The system of claim 1 wherein the first and second delay control cells each comprises a control transistor in parallel with a resistor, and each of the first and second delay times is produced by varying voltage levels of signals that control the control transistor in order to change channel widths of the control transistor.